WHAT IS CLAIMED IS:

1. An electronic device having a configurable port for connecting with a variety of interface device types, comprising:

a register for storing one or more sets of configuration data each set of configuration data corresponding to a particular interface device type that may be connected to the electronic device; and

a multiplexer for conforming a data signal in accordance with the configuration data associated with a particular interface device type connected to the electronic device.

2. The electronic device of Claim 1, wherein the interface device types include any of open drain interface type, open collector interface type, totem pole interface type, tri-state buffer interface type, and input types capable of being configured to detect active levels or edges.

3. The electronic device of Claim 1, wherein the data signal is an output data signal.

4. The electronic device of Claim 1, further comprising one or more load-enabled flip-flops for use as respective programmable registers.

5. The electronic device of Claim 4, wherein the flip-flops are implemented as D-type flip-flops.

6. The electronic device of Claim 4, wherein the load-enabled flip-flops include a first set of flip-flops for configuring and enabling signaling for the configurable port of the electronic device, and a second set of flip-flops for controlling input and output signaling for the configurable port.

7. The electronic device of Claim 1, wherein a controller controls the operation of the configurable port.

8. The electronic device of Claim 7, wherein the controller is associated with a register set for controlling the operation of the configurable port.

9. The electronic device of Claim 8, wherein the register set includes a first register for indicating whether the port is configured as a general purpose interface port or as a special purpose interface port to support a particular device connected with the port, a second register for configuring the port to transmit an output signal to the device connected with the port, a third register for indicating data representing the output signal to be transmitted to the device connected with the port, and a fourth register for indicating data representing an input signal that is received from the device connected with the port.

10. The electronic device of Claim 9, wherein the register set further includes a fifth register for indicating the status of the controller, a sixth register for indicating whether to enable an interrupt signal to interrupt a host processor, a seventh register for indicating an interrupt activation level, and an eighth register for clearing the contents of the fifth register.

11. The electronic device of Claim 8, wherein the register set includes one or more 8 bit registers.

12. The electronic device of Claim 4, further comprising an inbound buffer for buffering an input data signal from a device connected with the port, and an outbound buffer for buffering an output signal that conforms with an interface type of the device connected with the port.

13. The electronic device of Claim 4, further comprising an interruptable inbound buffer capable of individually enabling and disabling processor interrupts based on individual activity levels.

14. The electronic device of Claim 13, wherein the activity level is a high state activity level.

15. The electronic device of Claim 13, wherein the activity level is a low state activity level.

16. An electronic device having a configurable port for connecting with a variety of interface device types, comprising:

means for storing one or more sets of configuration data each set of configuration data corresponding to a particular interface device type that may be connected to the electronic device; and

means for conforming a data signal in accordance with the configuration data associated with a particular interface device type connected to the electronic device.

17. The electronic device of Claim 16, wherein the interface device types include any of open drain interface type, open collector interface type, totem pole interface type, and three state buffer interface type.

18. The electronic device of Claim 16, wherein the data signal is an output signal.

19. The electronic device of Claim 16, further comprising programmable register means for configuring the port in accordance with a particular interface device type.

20. The electronic device of Claim 19, wherein the programmable register means includes a means for configuring and enabling signaling for the configurable port of the electronic device, and a means for controlling input and output signaling for the configurable port.

21. The electronic device of Claim 16, wherein a controller controls the operation of the configurable port.

22. The electronic device of Claim 21, wherein the controller is associated with a means for controlling the operation of the configurable port.

23. The electronic device of Claim 22, wherein the controlling means includes a means for indicating whether the port is configured as a general purpose interface port or as a special purpose interface port to support a particular device connected with the port, a means for configuring the port to transmit an output signal to the device connected with the port, a means for indicating data representing the output signal to be transmitted to the device connected with

the port, and a means for indicating data representing an input signal that is received from the device connected with the port.

24. The electronic device of Claim 23, wherein the controlling means further includes a means for indicating the status of the controller, a means for indicating whether to enable an interrupt signal to interrupt a host processor, and a means for indicating an interrupt activation level.

25. The electronic device of Claim 16, further comprising a first buffering means for buffering an input data signal from a device connected with the port, and a second buffering means for buffering an output signal that conforms with an interface type of the device connected with the port.

26. The electronic device of Claim 16, further comprising an interruptable buffering means for individually enabling and disabling processor interrupts based on individual activity level.

27. The electronic device of Claim 26, wherein the activity level is a high state activity level.

28. The electronic device of Claim 26, wherein the activity level is a low state activity level.

29. A method for configuring a port to connect with a variety of interface device types, comprising the steps of:

storing one or more sets of configuration data relating to the variety of interface device types that may be connected to the electronic device, each set of configuration data corresponding to a particular interface device type;

configuring the port to interface with a particular one of the variety of interface device types; and

in response to enabling the port to transmit data to the connected device, conforming an output data signal in accordance with the configuration data associated with the particular interface device type connected to the electronic device;

in response to enabling the port to receive data from the connected device, receiving an input data signal and translating the input data signal as appropriate to interface with the port.

30. The method of Claim 29, wherein the interface device types include any of open drain interface type, open collector interface type, totem pole interface type, and three state buffer interface type.

31. The method of Claim 29, wherein the configuring step includes the steps of configuring and enabling signaling for the configurable port of the electronic device, and controlling input and output signaling for the configurable port.

32. The method of Claim 31, wherein the configuring step further includes providing a register set for controlling the operation of the configurable port, wherein the register set includes a first register for indicating whether the port is configured as a general purpose interface port or as a special purpose interface port to support a particular device connected with the port, a second register for configuring the port to transmit an output signal to the device connected with the port, a third register for indicating data representing the output signal to be transmitted to the device connected with the port, and a fourth register for indicating data representing an input signal that is received from the device connected with the port.

33. The method of Claim 32, wherein the register set further includes a fifth register for indicating the status of the controller, a sixth register for indicating whether to enable an interrupt signal to interrupt a host processor, a seventh register for indicating an interrupt activation level, and an eighth register for clearing the contents of the fifth register.

34. The method of Claim 29, further comprising the steps of buffering the input data signal from the device connected with the port in response to receiving the input data signal, and buffering the output signal that conforms with an interface type of the device connected with the port in response to transmitting the output signal to the device connected with the port.